

## M4i.22xx-x8 - 8 bit Digitizer up to 5 GS/s

- 5 GS/s on one channel
- 2.5 GS/s on two channels
- 1.25 GS/s on four channels
- up to 1.5 GHz bandwidth
- Ultra Fast PCI Express x8 Gen 2 interface
- Simultaneously sampling on all channels
- 4 input ranges:  $\pm 200$  mV up to  $\pm 2.5$  V
- Low voltage input range option  $\pm 40$  mV up to  $\pm 500$  mV
- Programmable input offset of  $\pm 200\%$
- 4 GSamples on-board memory
- Window, re-arm, OR/AND trigger
- Synchronization of up to 8 cards per system
- Features: Single-Shot, Streaming, Multiple Recording, Gated Sampling, ABA, Timestamps and optional Average and Statistics
- Direct data transfer to CUDA GPU using SCAPP option

Speed	SNR	ENOB
5 GS/s	>44.5 dB	>7.1 bit
2.5 GS/s	>45.6 dB	>7.3 bit
1.25 GS/s	>46.9 dB	>7.5 bit

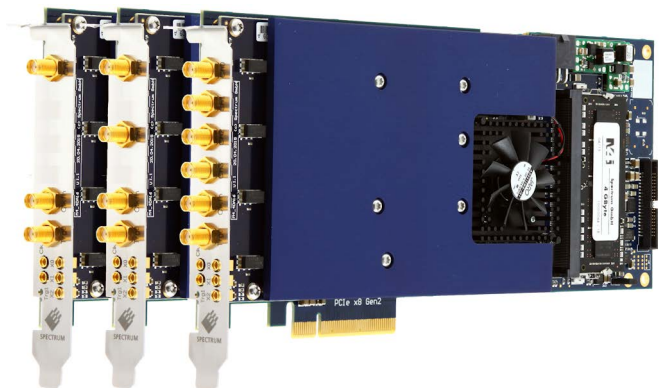
### FPGA Options:

- Block Average up to 128k
- Block Statistics/Peak Detect

**SCAPP**  
 Spectrum's CUDA Access – Parallel Processing

**M4i**  
 series

- PCIe x8 Gen 2 Interface
- Works with x8/x16 PCIe slots
- Sustained streaming mode more than 3.4 GB/s\*



### Operating Systems

- Windows 7 (SP1), 8, 10, 11  
Server 2008 R2 and newer
- Linux Kernel 3.x, 4.x, 5.x, 6.x
- Windows/Linux 32 and 64 bit

### Programming Languages

- C, C++, C#, Python
- Julia, Java, VB.NET, Delphi
- IVI

### Supported Software

- SBench 6
- MATLAB
- LabVIEW

Model	Bandwidth	1 channel	2 channels	4 channels
M4i.2234-x8	1.5 GHz	5 GS/s	2.5 GS/s	1.25 GS/s
M4i.2233-x8	1.5 GHz	5 GS/s	2.5 GS/s	
M4i.2230-x8	1.5 GHz	5 GS/s		
M4i.2221-x8	1.5 GHz	2.5 GS/s	2.5 GS/s	
M4i.2223-x8	1.5 GHz	2.5 GS/s	1.25 GS/s	
M4i.2220-x8	1.5 GHz	2.5 GS/s		
M4i.2212-x8	500 MHz	1.25 GS/s	1.25 GS/s	1.25 GS/s
M4i.2211-x8	500 MHz	1.25 GS/s	1.25 GS/s	
M4i.2210-x8	500 MHz	1.25 GS/s		

### General Information

The M4i.22xx-x8 series digitizers deliver the highest performance in both speed and resolution. The series includes PCIe cards with either one, two or four synchronous channels. The ADCs can sample at rates from 1.25 GS/s up to 5 GS/s with a maximum bandwidth of up to 1.5 GHz.

The digitizers feature a PCI Express x8 Gen 2 interface that offers outstanding data streaming performance. The interface and Spectrums optimized drivers enable data transfer rates in excess of 3.4 GB/s\*\* so that signals can be acquired, stored and analyzed at the fastest speeds. The cards are still software compatible with the drivers from earlier Spectrum digitizers starting with M2i series.

\*Throughput measured with a motherboard chipset supporting a TLP size of 256 bytes.

## Software Support

### Windows drivers

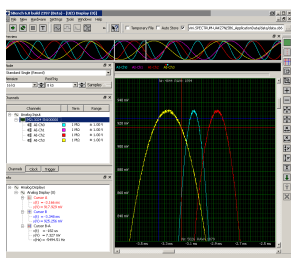
The cards are delivered with drivers for Windows 7, Windows 8 and Windows 10 (32 bit and 64 bit). Programming examples for Visual C++, C++ Builder, Delphi, Visual Basic, VB.NET, C#, Julia, Python, Java and IVI are included.

### Linux Drivers



All cards are delivered with full Linux support. Pre-compiled kernel modules are included for the most common distributions like Fedora, Suse, Ubuntu LTS or Debian. The Linux support includes SMP systems, 32 bit and 64 bit systems, versatile programming examples for GNU C++, Python and Julia, as well as the possibility to get the kernel driver sources for your own compilation.

### SBench 6



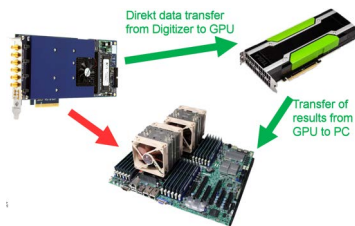
A base license of SBench 6, the easy-to-use graphical operating software for Spectrum cards, is included in the delivery. The base license makes it possible to test the card, display acquired data and make some basic measurements. It's a valuable tool for checking the card's performance and assisting with the unit's initial

setup. The cards also come with a demo license for the SBench 6 professional version. This license gives the user the opportunity to test the additional features of the professional version with their hardware. The professional version contains several advanced measurement functions, such as FFTs and X/Y display, import and export utilities as well as support for all acquisition modes including data streaming. Data streaming allows the cards to continuously acquire data and transfer it directly to the PC RAM or hard disk. SBench 6 has been optimized to handle data files of several GBytes. SBench 6 runs under Windows as well as Linux (KDE, GNOME and Unity) operating systems. A test version of SBench 6 can be downloaded directly over the internet and can run the professional version in a simulation mode without any hardware installed. Existing customers can also request a demo license for the professional version from Spectrum. More details on SBench 6 can be found in the SBench 6 data sheet.

### Third-party products

Spectrum supports the most popular third-party software products such as LabVIEW or MATLAB. All drivers come with detailed documentation and working examples are included in the delivery.

### SCAPP – CUDA GPU based data processing



For applications requiring high performance signal and data processing Spectrum offers SCAPP (Spectrum's CUDA Access for Parallel Processing). The SCAPP SDK allows a direct link between Spectrum digitizers, AWGs or Digital Data Acquisition

Cards and CUDA based GPU cards. Once in the GPU users can harness the processing power of the GPU's multiple (up to 10000) processing cores and large (up to 48 GB) memories. SCAPP uses an RDMA (Linux only) process to send data at the full PCIe transfer speed to and from the GPU card. The SDK includes a set of examples for interaction between the Spectrum card and the GPU card and another set of CUDA parallel processing examples with easy

building blocks for basic functions like filtering, averaging, data de-multiplexing, data conversion or FFT. All the software is based on C/C++ and can easily be implemented, expanded and modified with normal programming skills.

### Hardware features and options

#### PCI Express x8



The M4i series cards use a PCI Express x8 Gen 2 connection. They can be used in PCI Express x8 and x16 slots with Gen 1, Gen 2, Gen 3 or Gen4. The maximum

sustained data transfer rate is more than

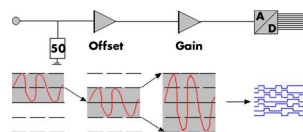
3.3 GByte/s (read direction) or 2.8 GByte/s (write direction) per slot. Server motherboards often recognize PCI Express x1, x2 or x4 connections in x8 or x16 slots. These slots can also be used with the M4i series cards but with reduced data transfer rates.

### Connections

- The cards are equipped with SMA connectors for the analog signals as well as for the external trigger and clock input. In addition, there are five MMCX connectors that are used for an additional trigger input, a clock output and three multi-function I/O connectors. These multi-function connectors can be individually programmed to perform different functions:
- Trigger output
- Status output (armed, triggered, ready, ...)
- Synchronous digital inputs, being stored inside the analog data samples
- Asynchronous I/O lines



### Input Amplifier



The analog inputs can be adapted to real world signals using a wide variety of settings that are individual for each channel. By using software commands one can select a matching input

range and the signal offset can be compensated by programmable AC coupling or offset shifting.

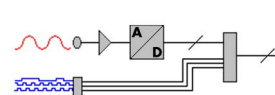
### Software selectable lowpass filter

Each analog channel contains a software selectable low-pass filter to limit the input bandwidth. Reducing the analog input bandwidth results in a lower total noise and can be useful especially with low voltage input signals.

### Automatic on-board calibration

Every channel of each card is calibrated in the factory before the board is shipped. However, to compensate for environmental variations like PC power supply, temperature and aging the software driver includes routines for automatic offset and gain calibration. This calibration is performed on all input ranges of the "Buffered" path and uses a high precision onboard calibration reference.

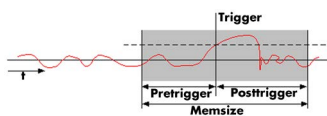
### Digital inputs



This option acquires additional synchronous digital channels phase-stable with the analog data. As standard a maximum of 3 additional

digital inputs are available on the front plate of the card using the multi-purpose I/O lines. An additional option offers 8 more digital channels.

## Ring buffer mode



The ring buffer mode is the standard mode of all oscilloscope instruments. Digitized data is continuously written into a ring memory until a trigger event is detected. After the trigger, post-trigger samples are recorded and pre-trigger samples can also be stored. The number of pre-trigger samples available simply equals the total ring memory size minus the number of post trigger samples.

## FIFO mode

The FIFO or streaming mode is designed for continuous data transfer between the digitizer card and the PC memory. When mounted in a PCI Express x8 Gen 2 interface read streaming speeds of up to 3.4 GByte/s are possible. The control of the data stream is done automatically by the driver on interrupt request basis. The complete installed onboard memory is used to buffer the data, making the continuous streaming process extremely reliable.

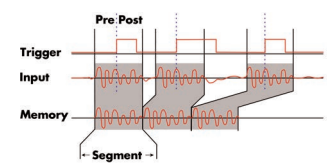
## Channel trigger

The digitizers offer a wide variety of trigger modes. These include a standard triggering mode based on a signals level and slope, like that found in most oscilloscopes. It is also possible to define a window mode, with two trigger levels, that enables triggering when signals enter or exit the window. Each input has its own trigger circuit which can be used to setup conditional triggers based on logical AND/OR patterns. All trigger modes can be combined with a re-arming mode for accurate trigger recognition even on noisy signals.

## External trigger input

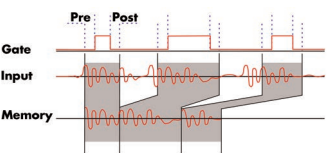
All boards can be triggered using up to two external analog or digital signals. One external trigger input has two analog comparators that can define an edge or window trigger, a hysteresis trigger or a rearm trigger. The other input has one comparator that can be used for standard edge and level triggers.

## Multiple Recording



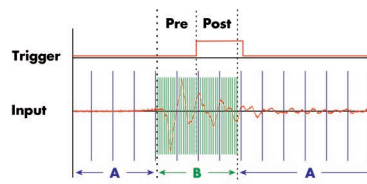
The Multiple Recording mode allows the recording of several trigger events with an extremely short re-arming time. The hardware doesn't need to be restarted in between. The on-board memory is divided in several segments of the same size. Each of them is filled with data if a trigger event occurs. Pre- and posttrigger of the segments can be programmed. The number of acquired segments is only limited by the used memory and is unlimited when using FIFO mode.

## Gated Sampling



The Gated Sampling mode allows data recording controlled by an external gate signal. Data is only recorded if the gate signal has a programmed level. In addition a pre-area before start of the gate signal as well as a post area after end of the gate signal can be acquired. The number of gate segments is only limited by the used memory and is unlimited when using FIFO mode.

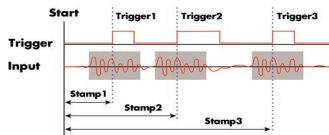
## ABA mode



The ABA mode combines slow continuous data recording with fast acquisition on trigger events. The ABA mode works like a slow data logger combined with a fast digitizer. The exact

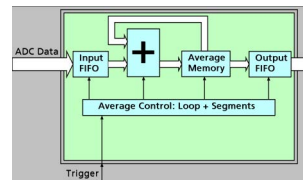
position of the trigger events is stored as timestamps in an extra memory.

## Timestamp



The timestamp function writes the time positions of the trigger events in an extra memory. The timestamps are relative to the start of recording, a defined zero time, externally synchronized to a radio clock, an IRIG-B or a GPS receiver. Using the external synchronization gives a precise time relation for acquisitions of systems on different locations.

## Firmware Option Block Average

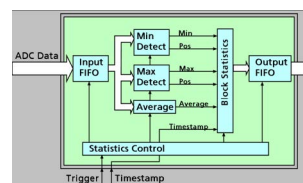


The Block Average Module improves the fidelity of noisy repetitive signals. Multiple repetitive acquisitions with very small dead-time are accumulated and averaged. Random noise is reduced by the averaging process improving

the visibility of the repetitive signal. The complete averaging process is done inside the FPGA of the digitizer generating no CPU load at all. The amount of data is greatly decreased as well as the needed transfer bandwidth is heavily reduced.

Please see separate data sheet for details on the firmware option.

## Firmware Option Block Statistics (Peak Detect)



The Block Statistics and Peak Detect Module implements a widely used data analysis and reduction technology in hardware. Each block is scanned for minimum and maximum peak and a summary including minimum, maximum, average, timestamps and position information is stored in memory. The complete averaging process is done inside the FPGA of the digitizer generating no CPU load at all. The amount of data is greatly decreased as well as the needed transfer bandwidth is heavily reduced.

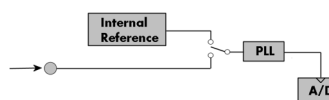
Please see separate data sheet for details on the firmware option.

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## External clock input and output

Using a dedicated connector a sampling clock can be fed in from an external system. Additionally it's also possible to output the internally used sampling clock on a separate connector to synchronize external equipment to this clock.

## Reference clock



The option to use a precise external reference clock (normally 10 MHz) is necessary to synchronize the instrument for high-quality measurements with external equipment (like a signal source). It's also possible to enhance the quality of the sampling clock in this

way. The driver automatically generates the requested sampling clock from the fed in reference clock.

## Star-Hub



The Star-Hub is an additional module allowing the phase stable synchronization of up to 8 boards of a kind in one system. Independent of the number of boards there is no phase delay between all channels. The Star-Hub distributes trigger and clock information between all boards to ensure all connected boards are running with the same clock and trigger. All trigger

sources can be combined with a logical OR allowing all channels of all cards to be the trigger source at the same time.

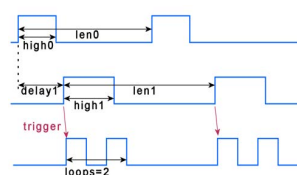
## External Amplifiers



For the acquisition of extremely small voltage levels with a high bandwidth a series of external amplifiers is available. Each of the one channel amplifiers is working with a fixed input impedance and allows - depending on the bandwidth - to select different amplification levels between x10 (20 dB) up to x1000 (60 dB). Us-

ing the external amplifiers of the SPA series voltage levels in the  $\mu\text{V}$  and mV area can be acquired.

## Firmware Option Digital Pulse Generator



The digital pulse generator option adds 4 internal independent digital pulse generators with programmable duty cycle, output frequency, delay and number of loops.

These digital pulse generators can be triggered by software, hardware trigger or can trigger

each other allowing to form complex pulse schemes to drive external equipment or experiments. The digital pulse generators can be output on the existing multi-XIO lines (X0, X1, ...) or can be used to trigger other pulse generators internally. Time resolution of the pulse generator depends on the cards type and the selected sampling rate and can be found in the technical data section.

The pulse generator option is a firmware option and can be later installed on all shipped cards.

## Technical Data



Only figures that are given with a maximum reading or with a tolerance reading are guaranteed specifications. All other figures are typical characteristics that are given for information purposes only. Figures are valid for products stored for at least 2 hours inside the specified operating temperature range, after a 30 minute warm-up, after running an on-board calibration and with proper cooled products. All figures have been measured in lab environment with an environmental temperature between 20°C and 25°C and an altitude of less than 100 m.

## Analog Inputs

Resolution  
Input Type  
ADC Differential non linearity (DNL)  
ADC Integral non linearity (INL)  
ADC Bit Error Rate (BER)  
Channel selection  
Analog Input impedance  
Input Ranges (standard ranges)  
Input Ranges (Low Voltage Option)  
Programmable Input Offset  
Input Coupling  
Max DC voltage if AC coupling active

ADC only  
ADC only  
sampling rate 1.25 GS/s  
software programmable  
fixed  
software programmable  
software programmable  
software programmable  
software programmable

8 Bit  
Single-ended  
 $\pm 0.35$  LSB  
 $\pm 0.9$  LSB  
 $10^{-16}$   
1, 2, or 4 (maximum is model dependent)  
50  $\Omega$   
 $\pm 200$  mV,  $\pm 500$  mV,  $\pm 1$  V,  $\pm 2.5$  V (programmable input offset at 0%)  
 $\pm 40$  mV,  $\pm 100$  mV,  $\pm 200$  mV,  $\pm 500$  mV (programmable input offset at 0%)  
 $\pm 200\%$  of input range (allowing bi-polar ranges to become uni-polar)  
AC/DC  
 $\pm 30$  V

Offset error (full speed)  
Gain error (full speed)  
Input offset error (full speed)  
Offset temperature drift  
Gain temperature drift  
Crosstalk 20 MHz sine signal (standard ranges)  
Crosstalk 20 MHz sine signal (standard ranges)  
Crosstalk 100 MHz sine signal (standard ranges)  
Crosstalk 100 MHz sine signal (standard ranges)

after warm-up and calibration  
after warm-up and calibration  
after warm-up and calibration  
after warm-up and calibration  
after warm-up and calibration  
 $\geq \pm 500$  mV standard range  
 $\geq \pm 200$  mV standard range  
 $\geq \pm 500$  mV standard range  
 $\geq \pm 200$  mV standard range

<0.5% of programmed input range  
<1% of input signal  
<2.5% of programmed input offset  
typical 5 ppm/°K  
typical 45 ppm/°K  
< -96 dB (all channel same input range)  
< -88 dB (all channel same input range)  
< -78 dB (all channel same input range)  
< -65 dB (all channel same input range)

Over voltage protection (standard ranges)

input range	$\pm 200$ mV	$\pm 500$ mV	$\pm 1$ V	$\pm 2.5$ V
max. continuous input power	22.5 dBm	27.0 dBm	27.0 dBm	27.0 dBm
max. peak input voltage	$\pm 3$ V	$\pm 7.5$ V	$\pm 15$ V	$\pm 30$ V

Over voltage protection (low voltage option)

input range	$\pm 40$ mV	$\pm 100$ mV	$\pm 200$ mV	$\pm 500$ mV
max. continuous input power	21.0 dBm	27.0 dBm	22.5 dBm	27.0 dBm
max. peak input voltage	$\pm 2.5$ V	$\pm 6.25$ V	$\pm 3$ V	$\pm 7.5$ V

Calibration	Internal	Self-calibration is done on software command and corrects against the on-board references. Self-calibration should be issued after warm-up time. <sup>A</sup>
Calibration	External	External calibration calibrates the on-board references used in self-calibration. All calibration constants are stored in non-volatile memory. A yearly external calibration is recommended.

## Trigger

Available trigger modes	software programmable	Channel Trigger, External, Software, Window, Re-Arm, Or/And, Delay, PXI (M4x only)
Channel trigger level resolution	software programmable	8 bit
Trigger engines		1 engine per channel with two individual levels, 2 external triggers
Trigger edge	software programmable	Rising edge, falling edge or both edges
Trigger delay	software programmable	0 to (8GSamples - 32) = 8589934560 Samples in steps of 32 samples
Multi, ABA, Gate: re-arming time	1.25 GS/s or below 2.5 GS/s 5 GS/s	80 samples (+ programmed pretrigger) 160 samples (+ programmed pretrigger) 320 samples (+ programmed pretrigger)
Pretrigger at Multi, ABA, Gate, FIFO	software programmable	32 up to 8192 Samples in steps of 32
Posttrigger	software programmable	32 up to 16G samples in steps of 32 (defining pretrigger in standard scope mode)
Memory depth	software programmable	64 up to [installed memory / number of active channels] samples in steps of 32
Multiple Recording/ABA segment size	software programmable	64 up to [installed memory / 2 / active channels] samples in steps of 32
Trigger accuracy (all sources)		1 sample
Timestamp modes	software programmable	Standard, Startreset, external reference clock on X0 (e.g. PPS from GPS, IRIG-B)
Data format		Std., Startreset: 64 bit counter, increments with sample clock (reset manually or on start) RefClock: 24 bit upper counter (increment with RefClock) 40 bit lower counter (increments with sample clock, reset with RefClock)
Extra data	software programmable	none, acquisition of X0/X1/X2 inputs at trigger time, trigger source (for OR trigger)
Size per stamp		128 bit = 16 bytes
External trigger		<b>Ext0</b> 50 Ω / 1 kΩ <b>Ext1</b> 1 kΩ
External trigger impedance	software programmable	AC or DC fixed DC
External trigger coupling	software programmable	Window comparator Single level comparator
External trigger type		±10 V (1 kΩ), ±2.5 V (50 Ω), ±10 V
External input level		2.5% of full scale range 2.5% of full scale range = 0.5 V
External trigger sensitivity (minimum required signal swing)		
External trigger level	software programmable	±10 V in steps of 10 mV ±10 V in steps of 10 mV
External trigger maximum voltage		±30V ±30 V
External trigger bandwidth DC	50 Ω 1 kΩ	n.a. DC to 200 MHz
External trigger bandwidth AC	50 Ω	20 kHz to 200 MHz n.a.
Minimum external trigger pulse width		≥ 2 samples ≥ 2 samples

## Clock

Clock Modes	software programmable	internal PLL, external reference clock, Star-Hub sync (M4i only), PXI Reference Clock (M4x only)
Internal clock accuracy		≤ ±20 ppm
Clock setup range	standard mode	all clock modes and all cards, single or synchronized by star-hub: maximum sampling clock 5 GS/s or 2.5 GS/s or 1.25 GS/s (depending on type) divider: maximum sampling rate divided by: 1, 2, 4, 8, 16, ... up to 262144
Clock setup range	special clock mode	internal clock only, single cards only, digitizerNETBOX with one internal digitizer only: maximum sampling clock 4 GS/s or 2 GS/s or 1 GS/s (depending on type) divider: maximum sampling rate divided by: 1, 2, 4, 8, 16, ... up to 262144
External reference clock range	software programmable	≥ 10 MHz and ≤ 1.25 GHz
External reference clock input impedance		50 Ω fixed
External reference clock input coupling		AC coupling
External reference clock input edge		Rising edge
External reference clock input type		Single-ended, sine wave or square wave
External reference clock input swing	square wave	0.3 V peak-peak up to 3.0 V peak-peak
External reference clock input swing	sine wave	1.0 V peak-peak up to 3.0 V peak-peak
External reference clock input max DC voltage		±30 V (with max 3.0 V difference between low and high level)
External reference clock input duty cycle requirement		45% to 55%
Clock setup granularity when using reference clock		divider: maximum sampling rate divided by: 1, 2, 4, 8, 16, ... up to 262144
Internal reference clock output type		Single-ended, AC-coupled, LVPECL, 750 mVpp (typical)
Internal reference clock output frequency		2.5 GHz / 64 = 39.0625 MHz
Star-Hub synchronization clock modes	software selectable	Internal clock (standard clock mode only), External reference clock
ABA mode clock divider for slow clock	software programmable	16 up to (128k - 16) in steps of 16
Channel to channel skew on one card		< 60 ps (typical)
Skew between star-hub synchronized cards		< 130 ps (typical, preliminary)

	M4i.223x / M4x.223x DN2.223-xx DN2.225-xx DN6.225-xx	M4i.222x / M4x.222x DN2.222-xx	M4i.221x / M4x.221x DN2.221-xx DN6.221-xx
ADC Resolution	8 bit	8 bit	8 bit
max sampling clock	5 GS/s	2.5 GS/s	1.25 GS/s
min sampling clock	4.768 kS/s	4.768 kS/s	4.768 kS/s
lower bandwidth limit (DC coupling)	0 Hz	0 Hz	0 Hz
lower bandwidth limit (AC coupling)	< 30 kHz	< 30 kHz	< 30 kHz
-3 dB bandwidth (no filter active), Standard input ranges	1.5 GHz	1.5 GHz	500 MHz-

	M4i.223x / M4x.223x DN2.223-xx DN2.225-xx DN6.225-xx	M4i.222x / M4x.222x DN2.222-xx	M4i.221x / M4x.221x DN2.221-xx DN6.221-xx
-3 dB bandwidth (no filter active), small input ranges, ir40m option installed	1.2 GHz	1.2 GHz	500 MHz-
-3 dB bandwidth (BW filter active)	~400 MHz	~400 MHz	~370 MHz

### **Block Average Signal Processing Option M4i.22xx/DN2.22x/DN6.22x Series**

		<b>Firmware ≥ V1.14 (since August 2015)</b>		<b>Firmware &lt; V1.14</b>
		<b>32 bit mode</b>	<b>16 bit mode</b>	
		64 samples	128 samples	32 bit mode only 64 samples
Data Mode (resulting sample width)	software programmable	32 samples	64 samples	32 samples
Minimum Waveform Length		64 kSamples	128 kSamples	32 kSamples
Minimum Waveform Stepsize		32 kSamples	64 kSamples	16 kSamples
Maximum Waveform Length	1 channel active	16 kSamples	32 kSamples	8 kSamples
Maximum Waveform Length	2 channels active	2	2	4
Maximum Waveform Length	4 or more channels active	16777216 (16M)	256	16777216 (16M)
Minimum Number of Averages				
Maximum Number of Averages				
Data Output Format	fixed	32 bit signed integer	16 bit signed integer	32 bit signed integer
Re-Arming Time between waveforms	1.25 GS/s or below	80 samples (+ programmed pretrigger)		80 samples (+ programmed pretrigger)
Re-Arming Time between waveforms	2.5 GS/s	160 samples (+ programmed pretrigger)		160 samples (+ programmed pretrigger)
Re-Arming Time between waveforms	5 GS/s	320 samples (+ programmed pretrigger)		320 samples (+ programmed pretrigger)
Re-Arming Time between end of average to start of next average		Depending on programmed segment length, max 50 µs		80/160/320 samples as above listed

### **Block Statistics Signal Processing Option M4i.22xx/DN2.22x Series/DN6.22x Series**

Minimum Waveform Length		64 samples
Minimum Waveform Stepsize		32 samples
Maximum Waveform Length	Standard Acquisition	2 GSamples / channels
Maximum Waveform Length	FIFO Acquisition	2 GSamples
Data Output Format	fixed	32 bytes statistics summary
Statistics Information Set per Waveform		Average, Minimum, Maximum, Position Minimum, Position Maximum, Trigger Timestamp
Re-Arming Time between Segments	1.25 GS/s or below	80 samples (+ programmed pretrigger)
Re-Arming Time between Segments	2.5 GS/s	160 samples (+ programmed pretrigger)
Re-Arming Time between Segments	5 GS/s	320 samples (+ programmed pretrigger)

### **Multi Purpose I/O lines (front-plate)**

Number of multi purpose lines		three, named X0, X1, X2
Input: available signal types	software programmable	Asynchronous Digital-In, Synchronous Digital-In, Timestamp Reference Clock
Input: impedance		10 kΩ to 3.3 V
Input: maximum voltage level		-0.5 V to +4.0 V
Input: signal levels		3.3 V LVTTTL (Low ≤ 0.8 V, High ≥ 2.0 V)
Input: bandwidth		125 MHz
Output: available signal types	software programmable	Asynchronous Digital-Out, Trigger Output, Run, Arm, PLL Refclock, System Clock
Output: impedance		50 Ω
Output: signal levels		3.3 V LVTTTL
Output: type		3.3V LVTTTL, TTL compatible for high impedance loads
Output: drive strength		Capable of driving 50 Ω loads, maximum drive strength ±48 mA
Output: update rate	14bit or 16 bit ADC resolution	sampling clock
Output: update rate	7 bit or 8 bit ADC resolution	Current sampling clock ≤ 1.25 GS/s : sampling clock Current sampling clock > 1.25 GS/s and ≤ 2.50 GS/s : ½ sampling clock Current sampling clock > 2.50 GS/s and ≤ 5.00 GS/s : ¼ sampling clock

### **Option M4i.xxxx-PulseGen**

Number of internal pulse generators	4
Number of pulse generator output lines	3 (Existing multi-purpose outputs X0 to X2)
Time resolution of pulse generator	Pulse generator's sampling rate is derived from instrument's sampling rate and value can be read out. Maximum possible pulse generator update rate is 22xx: 156.25 MS/s (6.4 ns) 23xx: 156.25 MS/s (6.4 ns) 44xx: 125.00 MS/s (8.0 ns) 66xx: 156.25 MS/s (6.4 ns)
Programmable output modes	Single-shot, multiple repetitions on trigger, gated
Programmable trigger sources	Software, Card Trigger, Other Pulse Generator, XIO lines.
Programmable trigger gate	None, ARM state, RUN state
Programmable length (frequency)	2 to 4G samples in steps of 1 (32 bit)
Programmable width (duty cycle)	1 to 4G samples in steps of 1 (32 bit)
Programmable delay	0 to 4G samples in steps of 1 (32 bit)
Programmable loops	0 to 4G samples in steps of 1 (32 bit) - 0 = infinite
Output level of digital pulse generators	Please see section of multi-purpose I/O lines



## Dynamic Parameters

<b>M4i.223x, M4x.223x and DN2.223-xx, DN2.225-xx and DN6.225-xx, 8 Bit 5 GS/s</b>												
DC or AC coupled, fixed 50 Ohm												
Input Path	10 MHz				40 MHz		70 MHz		240 MHz		600 MHz	
Test signal frequency												
Input Range	±200 mV	±500 mV	±1 V	±2.5 V	±200 mV	±1V	±200 mV	±1V	±200 mV	±1V	±200 mV	±1V
THD (typ) (dB)	<60.2 dB	<60.3 dB	<60.3 dB	<60.3 dB	<58.9 dB	<58.2 dB	<58.8 dB	<58.0 dB	<54.0 dB	<54.0 dB	<45.0 dB	<46.3 dB
SNR (typ) (dB)	>44.5 dB	>44.8 dB	>44.8 dB	>44.5 dB	>44.7 dB	>44.7 dB	>44.3 dB	>44.3 dB	>42.9 dB	>42.9 dB	>40.3 dB	>40.2 dB
SFDR (typ), excl. harm. (dB)	>53.7 dB	>54.9 dB	>54.9 dB	>54.2 dB	>50.3 dB	>50.8 dB	>50.2 dB	>49.7 dB	>49.4 dB	>49.5 dB	>44.3 dB	>44.6 dB
SFDR (typ), incl. harm. (dB)	>53.7 dB	>54.7 dB	>54.8 dB	>54.2 dB	>50.3 dB	>50.8 dB	>50.2 dB	>49.7 dB	>49.4 dB	>49.5 dB	>44.3 dB	>44.6 dB
SINAD/THD+N (typ) (dB)	>44.4 dB	>44.7 dB	>44.7 dB	>44.4 dB	>44.5 dB	>44.4 dB	>44.2 dB	>44.1 dB	>42.6 dB	>42.6 dB	>39.1 dB	>39.3 dB
ENOB based on SINAD (bit)	>7.1 bit	>7.1 bit	>7.1 bit	>7.1 bit	>7.1 bit	>7.1 bit	>7.1 bit	>7.0 bit	>6.8 bit	>6.8 bit	>6.2 bit	>6.2 bit
ENOB based on SNR (bit)	>7.1 bit	>7.1 bit	>7.1 bit	>7.1 bit	>7.1 bit	>7.1 bit	>7.1 bit	>7.1 bit	>6.9 bit	>6.9 bit	>6.4 bit	>6.4 bit

<b>M4i.222x, M4x.222x and DN2.222-xx, 8 Bit 2.5 GS/s</b>												
DC or AC coupled, fixed 50 Ohm												
Input Path	10 MHz				40 MHz		70 MHz		240 MHz		600 MHz	
Test signal frequency												
Input Range	±200 mV	±500 mV	±1 V	±2.5 V	±200 mV	±1V	±200 mV	±1V	±200 mV	±1V	±200 mV	±1V
THD (typ) (dB)	>56.2 dB	<56.3 dB	<56.5 dB	<56.4 dB	<55.9 dB	<55.9 dB	<54.9 dB	<55.3 dB	<53.9 dB	<53.4 dB	<43.9 dB	<45.2 dB
SNR (typ) (dB)	>45.6 dB	>45.8 dB	>45.6 dB	>45.5 dB	>44.7 dB	>44.9 dB	>44.5 dB	>44.6 dB	>43.9 dB	>44.0 dB	>42.1 dB	>41.9 dB
SFDR (typ), excl. harm. (dB)	>57.2 dB	>57.3 dB	>55.7 dB	>55.1 dB	>50.9 dB	>50.5 dB	>50.9 dB	>50.6 dB	>49.8 dB	>49.0 dB	>46.3 dB	>45.2 dB
SFDR (typ), incl. harm. (dB)	>56.5 dB	>56.3 dB	>55.1 dB	>54.5 dB	>50.9 dB	>50.5 dB	>50.9 dB	>50.6 dB	>49.8 dB	>49.0 dB	>45.2 dB	>45.2 dB
SINAD/THD+N (typ) (dB)	>45.2 dB	>45.4 dB	>45.3 dB	>45.2 dB	>44.4 dB	>44.4 dB	>44.2 dB	>44.3 dB	>43.5 dB	>43.5 dB	>39.9 dB	>40.2 dB
ENOB based on SINAD (bit)	>7.2 bit	>7.3 bit	>7.2 bit	>7.2 bit	>7.1 bit	>7.1 bit	>7.1 bit	>7.1 bit	>6.9 bit	>6.9 bit	>6.3 bit	>6.4 bit
ENOB based on SNR (bit)	>7.3 bit	>7.3 bit	>7.3 bit	>7.3 bit	>7.1 bit	>7.1 bit	>7.1 bit	>7.1 bit	>7.0 bit	>7.0 bit	>6.7 bit	>6.7 bit

<b>M4i.221x, M4x.221x, DN2.221 and DN6.221-xx, 8 Bit 1.25 GS/s - standard input ranges</b>												
DC or AC coupled, fixed 50 Ohm												
Input Path	10 MHz				40 MHz		70 MHz		240 MHz			
Test signal frequency												
Input Range	±200 mV	±500 mV	±1 V	±2.5 V	±200 mV	±1V	±200 mV	±1V	±200 mV	±1V		
THD (typ) (dB)	<59.0 dB	<58.9 dB	<58.9 dB	<59.0 dB	<53.6 dB	<53.2 dB	<54.4 dB	<54.6 dB	<52.1 dB	<52.4 dB		
SNR (typ) (dB)	>46.9 dB	>47.0 dB	>47.0 dB	>47.0 dB	>46.8 dB	>47.0 dB	>47.0 dB	>47.0 dB	>46.1 dB	>46.2 dB		
SFDR (typ), excl. harm. (dB)	>62.1 dB	>62.1 dB	>62.2 dB	>62.0 dB	>58.2 dB	>59.8 dB	>62.2 dB	>61.9 dB	>59.5 dB	>58.5 dB		
SFDR (typ), incl. harm. (dB)	>60.7 dB	>60.4 dB	>60.5 dB	>60.4 dB	> 56.1 dB	>56.2 dB	> 57.7 dB	>57.6 dB	>52.5 dB	>52.7 dB		
SINAD/THD+N (typ) (dB)	>46.6 dB	>46.7 dB	>46.7 dB	>46.7 dB	>46.0 dB	>46.1 dB	>46.3 dB	>46.3 dB	>45.1 dB	>45.3 dB		
ENOB based on SINAD (bit)	>7.5 bit	>7.5 bit	>7.5 bit	>7.5 bit	>7.4 bit	>7.4 bit	>7.4 bit	>7.4 bit	>7.2 bit	>7.2 bit		
ENOB based on SNR (bit)	>7.5 bit	>7.5 bit	>7.5 bit	>7.5 bit	>7.5 bit	>7.5 bit	>7.5 bit	>7.5 bit	>7.3 bit	>7.4 bit		

<b>M4i.221x, M4x.221x and DN2.221-xx, 8 Bit 1.25 GS/s - low voltage input ranges</b>												
DC or AC coupled, fixed 50 Ohm												
Input Path	10 MHz				40 MHz		70 MHz		240 MHz			
Test signal frequency												
Input Range	±40 mV	±100 mV	±200 mV	±500 mV	±40 mV	±100 mV	±40 mV	±100 mV	±40 mV	±100 mV		
THD (typ) (dB)	<57.0 dB	<57.0 dB	<57.1 dB	<57.2 dB								
SNR (typ) (dB)	>44.0 dB	>44.9 dB	>44.9 dB	>44.9 dB								
SFDR (typ), excl. harm. (dB)	>62.1 dB	>62.1 dB	>62.1 dB	>62.2 dB								
SFDR (typ), incl. harm. (dB)	>60.1 dB	>60.2 dB	>60.2 dB	>60.4 dB								
SINAD/THD+N (typ) (dB)	>44.0 dB	>44.8 dB	>44.8 dB	>44.8 dB								
ENOB based on SINAD (bit)	>7.0 bit	>7.2 bit	>7.2 bit	>7.2 bit								
ENOB based on SNR (bit)	>7.0 bit	>7.2 bit	>7.2 bit	>7.2 bit								

Dynamic parameters are measured at ±1 V input range (if no other range is stated) and 50Ω termination with the samplerate specified in the table. Measured parameters are averaged 20 times to get typical values. Test signal is a pure sine wave generated by a signal generator and a matching bandpass filter. Amplitude is >99% of FSR. SNR and RMS noise parameters may differ depending on the quality of the used PC. SNR = Signal to Noise Ratio, THD = Total Harmonic Distortion, SFDR = Spurious Free Dynamic Range, SINAD = Signal Noise and Distortion, ENOB = Effective Number of Bits.

## RMS Noise Level (Zero Noise)

M4i.223x, M4x.223x and DN2.223-xx, DN2.225-xx, DN6.225-xx, 8 Bit 5 GS/s								
Input Range	±200 mV		±500 mV		±1		±2.5 V	
Voltage resolution (1 LSB)	1.6 mV		3.9 mV		7.8 mV		19.5 mV	
DC, fixed 50 Ω, typical	<0.3 LSB	<0.5 mV	<0.3 LSB	<1.2 mV	<0.3 LSB	<2.3 mV	<0.3 LSB	<5.9 mV
DC, fixed 50 Ω, maximum	<0.6 LSB	<0.9 mV	<0.6 LSB	<2.3 mV	<0.5 LSB	<4.7 mV	<0.5 LSB	<11.7 mV
M4i.222x, M4x.222x and DN2.222-xx, 8 Bit 2.5 GS/s								
Input Range	±200 mV		±500 mV		±1		±2.5 V	
Voltage resolution (1 LSB)	1.6 mV		3.9 mV		7.8 mV		19.5 mV	
DC, fixed 50 Ω, typical	<0.3 LSB	<0.5 mV	<0.3 LSB	<1.2 mV	<0.3 LSB	<2.3 mV	<0.3 LSB	<5.9 mV
DC, fixed 50 Ω, maximum	<0.6 LSB	<0.9 mV	<0.7 LSB	<2.7 mV	<0.5 LSB	<4.7 mV	<0.5 LSB	<11.7 mV
Standard Version								
M4i.221x, M4x.221x and DN2.221-xx, 8 Bit 1.25 GS/s								
Input Range	±200 mV		±500 mV		±1		±2.5 V	
Voltage resolution (1 LSB)	1.6 mV		3.9 mV		7.8 mV		19.5 mV	
DC, fixed 50 Ω, typical	<0.2 LSB	<0.3 mV	<0.2 LSB	<0.8 mV	<0.2 LSB	<1.6 mV	<0.2 LSB	<3.9 mV
DC, fixed 50 Ω, maximum	<0.3 LSB	<0.5 mV	<0.3 LSB	<1.2 mV	<0.3 LSB	<2.3 mV	<0.3 LSB	<5.9 mV
Low Voltage Version								
M4i.221x, M4x.221x and DN2.221-xx, 8 Bit 1.25 GS/s								
Input Range	±40 mV		±100 mV		±200 mV		±500 mV	
Voltage resolution (1 LSB)	0.3 mV		0.8 mV		1.6 mV		3.9 mV	
DC, fixed 50 Ω, typical	<0.4 LSB	<0.2 mV	<0.4 LSB	<0.3 mV	<0.4 LSB	<0.6 mV	<0.4 LSB	<1.6 mV
DC, fixed 50 Ω, maximum	<0.5 LSB	<0.2 mV	<0.5 LSB	<0.4 mV	<0.5 LSB	<0.8 mV	<0.5 LSB	<2.0 mV

## Connectors

Analog Inputs/Analog Outputs	SMA female (one for each single-ended input)	Cable-Type: Cab-3mA-xx-xx
Trigger 0 Input	SMA female	Cable-Type: Cab-3mA-xx-xx
Clock Input	SMA female	Cable-Type: Cab-3mA-xx-xx
Trigger 1 Input	MMCX female	Cable-Type: Cab-1m-xx-xx
Clock Output	MMCX female	Cable-Type: Cab-1m-xx-xx
Multi Purpose I/O	MMCX female (3 lines)	Cable-Type: Cab-1m-xx-xx

## Connection Cycles

All connectors have an expected lifetime as specified below. Please avoid to exceed the specified connection cycles or use connector savers.

SMA connector	500 connection cycles
MMCX connector	500 connection cycles
PCIe connector	50 connection cycles
PCIe power connector	30 connection cycles

## Environmental and Physical Details

Dimension (Single Card)	L x H x W: 241 mm (¾ PCIe length) x 107 mm x 20 mm (single slot width)
Dimension (Card with option SH8tm installed)	241 mm (¾ PCIe length) x 107 mm x 40 mm (double slot width, extends W by 1 slot right of the main card's bracket, on „component side“ of the PCIe card.)
Dimension (Card with option SH8ex installed)	Extends L to 312 mm (full PCIe length) x 107 mm x 20 mm (single slot width)
Dimension (Card with option M4i.44xx-DigSMA installed)	241 mm (¾ PCIe length) x 107 mm x 40 mm (double slot width, extends W by 1 slot left of the main card's bracket, on „solder side“ of the PCIe card.)
Weight (M4i.44xx series)	maximum 290 g
Weight (M4i.22xx, M4i.23xx, M4i.66xx, M4i.77xx series)	maximum 420 g
Weight (Option star-hub -sh8ex, -sh8tm)	including 8 sync cables 130 g
Weight (Option M4i.44xx-DigSMA)	320 g
Warm up time	10 minutes
Operating temperature	0°C to 50°C
Storage temperature	-10°C to 70°C
Humidity	10% to 90%
Dimension of packing	1 or 2 cards 470 mm x 250 mm x 130 cm
Volume weight of packing	1 or 2 cards 4 kg

## PCI Express specific details

PCIe slot type	x8 Generation 2 (Gen2)
PCIe slot compatibility (physical)	x8/x16
PCIe slot compatibility (electrical)	x1, x2, x4, x8, x16 with PCIe Gen1, Gen2, Gen3, Gen4 or Gen5
Sustained streaming mode (Card-to-System): M4i.22xx, M4i.23xx, M4i.44xx, M4i.77xx	> 3.4 GB/s
Sustained streaming mode (System-to-Card): M4i.66xx	(measured with a chipset supporting a TLP size of 256 bytes, using PCIe x8 Gen2)
	> 2.8 GB/s
	(measured with a chipset supporting a TLP size of 256 bytes, using PCIe x8 Gen2)



## Certification, Compliance, Warranty

According to EN ISO/IEC 17050-1:2010  
EMC Compliance

Safety Compliance

RoHS Compliance

REACH Compliance  
Product warranty  
Software and firmware updates

Compliant with CE Mark  
Electromagnetic Compatibility Directive 2014/30/EU (EMC)  
Applied Standards:  
EN 55032: 2016 (CISPR 32)  
EN 61000-4-2: 2009 (IEC 61000-4-2)  
EN 61000-4-3: 2011 (IEC 61000-4-3)

Compliant with CE Mark  
Low Voltage Directive 2014/35/EU (LVD)  
Applied Standards:  
IEC 61010-1: 2010 / EN 61010-1: 2010

RoHS Directive 2015/863/EC  
RoHS Directive 2011/65/EC (RoHS II)  
RoHS Directive 2002/95/EC (RoHS)  
REACH directive 2006/1907/EC  
5 years starting with the day of delivery  
Life-time, free of charge

## Power Consumption

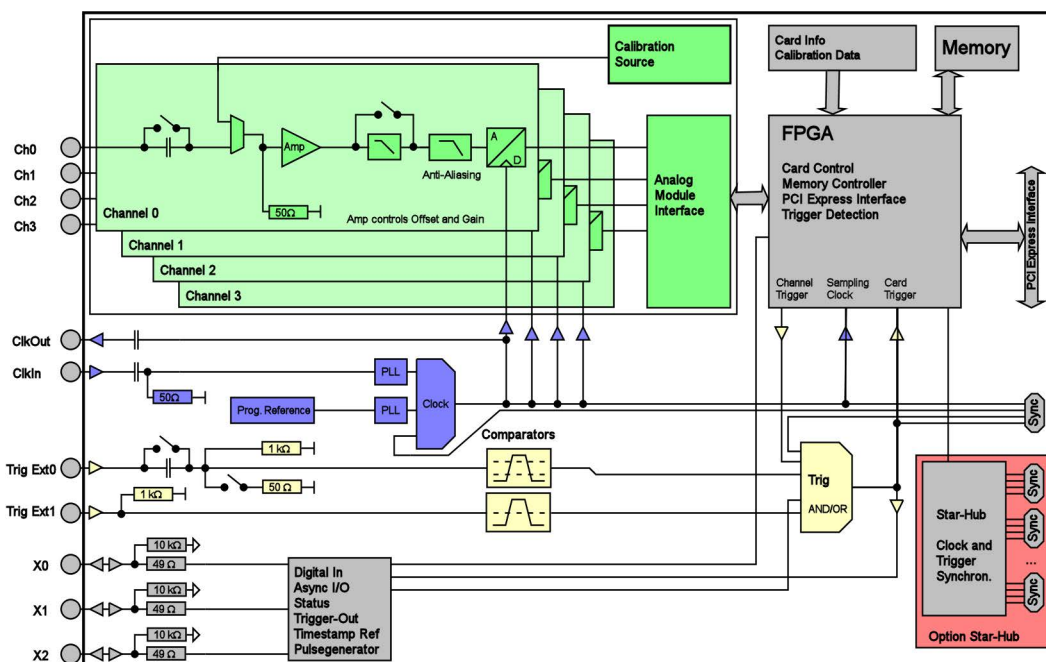
	PCI EXPRESS		
	3.3V	12 V	Total
M4i.2230-x8, M4i.2220-x8, M4i.2210-x8	0.2 A	2.6 A	32 W
M4i.2233-x8, M4i.2221-x8, M4i.2223-x8, M4i.2211-x8	0.2 A	2.7 A	33 W
M4i.2234-x8, M4i.2212-x8	0.2 A	2.9 A	35 W

## MTBF

MTBF

200000 hours

## Hardware block diagram



## Order Information

The card is delivered with 4 GSample on-board memory and supports standard acquisition (Scope), FIFO acquisition (streaming), Multiple Recording, Gated Sampling, ABA mode and Timestamps. Operating system drivers for Windows/Linux 32 bit and 64 bit, examples for C/C++, LabVIEW (Windows), MATLAB (Windows and Linux), IVI, .NET, Delphi, Java, Python, Julia and a Base license of the oscilloscope software SBench 6 are included.

**Adapter cables are not included. Please order separately!**

## PCI Express x8

Order no.	Bandwidth Standard	Bandwidth ir40m option	Standard mem	1 channel	2 channels	4 channels
M4i.2210-x8	500 MHz	500 MHz	4 GSample	1.25 GS/s		
M4i.2211-x8	500 MHz	500 MHz	4 GSample	1.25 GS/s	1.25 GS/s	
M4i.2212-x8	500 MHz	500 MHz	4 GSample	1.25 GS/s	1.25 GS/s	1.25 GS/s
M4i.2220-x8	1.5 GHz	1.2 GHz	4 GSample	2.5 GS/s		
M4i.2221-x8	1.5 GHz	1.2 GHz	4 GSample	2.5 GS/s	2.5 GS/s	
M4i.2223-x8	1.5 GHz	1.2 GHz	4 GSample	2.5 GS/s	1.25 GS/s	
M4i.2230-x8	1.5 GHz	1.2 GHz	4 GSample	5 GS/s		
M4i.2233-x8	1.5 GHz	1.2 GHz	4 GSample	5 GS/s	2.5 GS/s	
M4i.2234-x8	1.5 GHz	1.2 GHz	4 GSample	5 GS/s	2.5 GS/s	1.25 GS/s

## Options

Order no.	Option
M4i.22xx-ir40m	Low voltage input range option for 22xx series. 4 Input ranges with $\pm 40$ mV, $\pm 100$ mV, $\pm 200$ mV, $\pm 500$ mV, bandwidth limited.

## Options

Order no.	Option
M4i.xxxx-SH8ex <sup>(1)</sup>	Synchronization Star-Hub for up to 8 cards (extension), only one slot width, extension of the card to full PCI Express length (312 mm). 8 synchronization cables included.
M4i.xxxx-SH8tm <sup>(1)</sup>	Synchronization Star-Hub for up to 8 cards (top mount), two slots width, top mounted on card. 8 synchronization cables included.
M4i-upgrade	Upgrade for M4i.xxxx: Later installation of option Star-Hub

## Firmware Options

Order no.	Option
M4i.xxxx-spavg	Signal Processing Firmware Option: Block Average (later firmware-upgrade available)
M4i.xxxx-spstat	Signal Processing Firmware Option: Block Statistics/Peak Detect (later firmware-upgrade available)
M4i.xxxx-PulseGen	Firmware Option: adds 4 freely programmable digital pulse generators that use the XIO lines for output (later installation by firmware-upgrade available)

## Services

Order no.	
Recal	Recalibration at Spectrum incl. calibration protocol

## Standard Cables

for Connections	Length	Order no.				
		to BNC male	to BNC female	to SMA male	to SMA female	to SMB female
Analog/Clock-In/Trig-In	80 cm	Cab-3mA-9m-80	Cab-3mA-9f-80	Cab-3mA-3mA-80		Cab-3f-3mA-80
Analog/Clock-In/Trig-In	200 cm	Cab-3mA-9m-200	Cab-3mA-9f-200	Cab-3mA-3mA-200		Cab-3f-3mA-200
Probes (short)	5 cm		Cab-3mA-9f-5			
Clk-Out/Trig-Out/Extra	80 cm	Cab-1m-9m-80	Cab-1m-9f-80	Cab-1m-3mA-80	Cab-1m-3fA-80	Cab-1m-3f-80
Clk-Out/Trig-Out/Extra	200 cm	Cab-1m-9m-200	Cab-1m-9f-200	Cab-1m-3mA-200	Cab-1m-3fA-200	Cab-1m-3f-200
Information	The standard adapter cables are based on RG174 cables and have a nominal attenuation of 0.3 dB/m at 100 MHz and 0.5 dB/m at 250 MHz. For high speed signals we recommend the low loss cables series CHF					

## Low Loss Cables

Order No.	Option
CHF-3mA-3mA-200	Low loss cables SMA male to SMA male 200 cm
CHF-3mA-9m-200	Low loss cables SMA male to BNC male 200 cm
Information	The low loss adapter cables are based on MF141 cables and have an attenuation of 0.3 dB/m at 500 MHz and 0.5 dB/m at 1.5 GHz. They are recommended for signal frequencies of 200 MHz and above.

## Amplifiers

Order no.	Bandwidth	Connection	Input Impedance	Coupling	Amplification
SPA.1841 <sup>(2)</sup>	2 GHz	SMA	50 Ohm	AC	x100 (40 dB)
SPA.1801 <sup>(2)</sup>	2 GHz	SMA	50 Ohm	AC	x10 (20 dB)
SPA.1601 <sup>(2)</sup>	500 MHz	BNC	50 Ohm	DC	x10 (20 dB)
Information	External Amplifiers with one channel, BNC/SMA female connections on input and output, manually adjustable offset, manually switchable settings. An external power supply for 100 to 240 VAC is included. Please be sure to order an adapter cable matching the amplifier connector type and matching the connector type for your A/D card input.				

## Software SBench6

Order no.	
SBench6	Base version included in delivery. Supports standard mode for one card.
SBench6-Pro	Professional version for one card: FIFO mode, export/import, calculation functions
SBench6-Multi	Option multiple cards: Needs SBench6-Pro. Handles multiple synchronized cards in one system.
Volume Licenses	Please ask Spectrum for details.

## Software Options

Order no.	
SPc-RServer	Remote Server Software Package - LAN remote access for M2i/M3i/M4i/M4x/M2p/M5i cards
SPc-SCAPP	Spectrum's CUDA Access for Parallel Processing - SDK for direct data transfer between Spectrum card and CUDA GPU. Includes RDMA activation and examples.

<sup>(1)</sup> : Just one of the options can be installed on a card at a time.

<sup>(2)</sup> : Third party product with warranty differing from our export conditions. No volume rebate possible.

### Technical changes and printing errors possible

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